PART NUMBER	PACKAGE MARKING	PACKAGE DISCRIPTION
SCT63140FMA(1)	3140	QFN-15L

(1) For Tape & Reel, Add Suffix R (e.g. SCT63140FMAR)

Over operating free-air temperature unless otherwise noted(1)

DESCRIPTION	MIN	MAX	UNIT
VIN	-0.3	24	V
PVIN1, PVIN2	-0.3	17	V
SW1,SW2	-1	17	V
BST1,BST2	-0.3	23	V
BST1-SW1,BST2-SW2	-0.3	6	V
VDD, V3P3, ISNS, EN PWM1, PWM2	-0.3	6	V
Operating junction temperature TJ(2)	-40	125	°C
Storage temperature TSTG	-65	150	°C

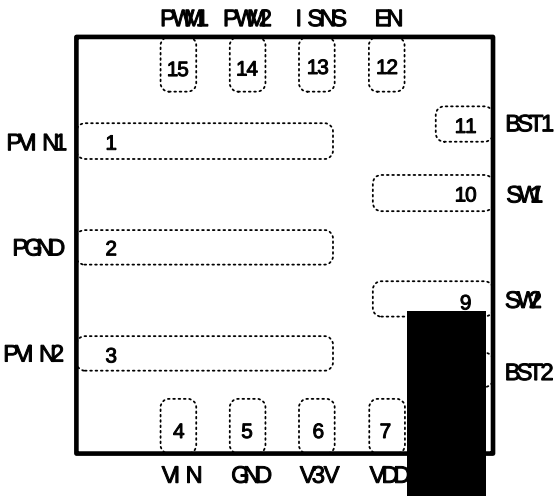


Figure 1. Top view 15-Lead QFN 3 mm

(1) Stresses beyond those listed under Absolute Maximum Rating may cause device permanent damage. The device is not teed to function outside of its Recommended Operation Conditions.
(2) The IC includes over temperature protection to protect the device during overload conditions. Junction temperature will 150°C when over temperature protection is active. Continuous operation above the specified maximum operating junction temp will reduce lifetime.

NAME	NO.	PIN FUNCTION
PVIN1	1	Input supply voltage of half-bridge FETs Q1 and Q2. Connected to nditi u49.5 46

V_{PVIN1}=V_{PIN2}=12V, VDD=5V, typical value is tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Input supplies and UVLO						
V_{IN}	Operating input voltage		4.2		20	V
P_{VIN}	Operating input voltage		1		15	V
V_{IN_UVLO}	V_{IN} UVLO Threshold Hysteresis	V_{IN} rising		3.6 400		V mV
V_{DD_UVLO}	V_{DD} UVLO Threshold Hysteresis	V_{DD} rising		3.8 440		V mV
I_{SHDN}	Shutdown current from VIN pin	EN=0V, VIN=12V		1	3	A
I_{SHDN_PVIN}	Shutdown current from PVIN1,PVIN2	EN=0V, PVIN=12V		1	3	uA
I_{VINQ}	Quiescent current from VIN pin	EN floating, VDD=5V, no loading on LDO		300		uA
I_{PVINQ}	Quiescent current from PVIN1, PVIN2	EN floating, VDD=5V, no loading on LDO		50		uA
ENABLE INPUTS and PWM logic						
V_{EN_H}	Enable high threshold			1.18		V
V_{EN_L}	Enable low threshold			1.1		V
V_{IH}	PWM1, PWM2 Logic level high	V3P3=3.3V, VDD=5V	2.65			V
V_{IL}	PWM1, PWM2 Logic level low	V3P3=3.3V, VDD=5V			0.55	V
V_{TS}	PWM1, PWM2 Tri-state voltage		1.2		2	V
Power Stage						
$R_{DSON\_Q1\ Q3}$	High-side MOSFET Q1 Q3 on-resistance	V_{BST1}-V_{SW1}=5V, V_{BST2}-V_{SW2}=5V		16		m
$R_{DSON\_Q2\ Q4}$	Low-side MOSFET Q2 Q4 on-resistance	VDD=5V		16		m
I_{LIM}	High-side current limit threshold			12.5		A
5V LDO						
V_{DD}	Output voltage	Cout=10uF	4.95	5	5.05	V
I_{DD}	Output current Capability			100		mA
3.3V LDO						
V_{3P3}	Output voltage	Cout=1uF, VDD=5V	3.267	3.3	3.333	V
I_{3P3}	Output current Capability	VDD=5V		100		mA
I_{SC}	Short current			50		mA
Current Sense						
V_{ISNS0}	Voltage with no input current	I_{PGND}=0A ,Tj=25 PWM1=PWM2=0V	0.585	0.6	0.615	V
R_{ISNS}	Input current to output voltage gain	V_{ISNS}=V_{ISNS0}+I_{PGND}*R_{ISNS}	0.98	1	1.02	V/A
V_{ISNS1}	Voltage with 0.6A input current	I_{PVIN}=0.6A, Tj=25	1.176	1.2	1.224	V
V_{ISNS2}	Voltage with 1A input current	I_{PVIN}=1A, Tj=25	1.568	1.6	1.632	V
Protection						
T_{SD}	Thermal shutdown threshold Hysteresis	T_J rising		155 35		°C °C

Overview

The SCT63140 is a highly integrated power management unit optimized for wireless power transmitter applications. This device integrates the power functions required to a wireless power transmitter including 5V output LDO as power supply for external transmitter controller, full bridge power stage to convert DC input power to AC output for driving LC resonant circuit, lossless current sensing with ±2% accuracy, 3.3V output LDO for powering MCU.

The SCT63140 has three power input pins. VIN is connected to the power FETs of 5V LDO. PVIN1 and PVIN2 are connected to the power FETs of the full bridge and conducts high currents for power transfer.

VIN and PVIN1, PVIN2 can be powered separately for more flexibility of system power design. The operating voltage range for VIN is from 4.2V to 20V. An Under-voltage Lockout(UVLO) circuit monitors the voltage of VIN pin and disable the IC operation when VIN voltage falls below the UVLO threshold of 3.2V typically. The maximum operating voltage for PVIN is up to 15V while the minimum voltage accepted can be down to 1V. Another UVLO circuit also supervise the VDD voltage which is the power supply for gate drivers of full bridge MOSFETs. Full bridge will work when VDD UVLO release.

Two independent PWM signals control two separate half bridge MOSFETs with internal adaptive non-overlap circuitry to prevent the shoot-through of MOSFETs in each bridge. PWM logics are compatible for both 3.3V and 5V IOs so the SCT63140 can accept PWM signal from the controller with using either 3.3V or 5V power supply.

The full bridge of power MOSFETs includes proprietary designed gate driver scheme to resist switching node ringing without sacrificing MOSFET turn-on and turn-off time, which further erases high frequency radiation EMI noise caused by the MOSFETs hard switching. This allows the user to reduce the system cost and design effort for EMI reduction.

The SCT63140 full protection features include VIN and VDD under-voltage lockout, over current protection with cycle-by-cycle current limit and hiccup mode, output hard short protection for 4-MOSFETs full bridge, current limit and current fold back at hard short for two LDOs and whole chip thermal shutdown protection.

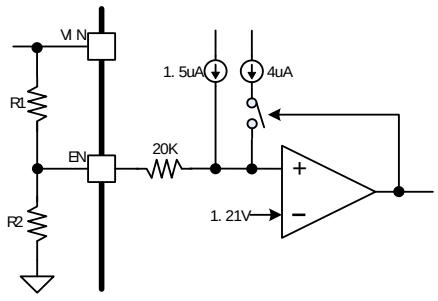
Enable and Start up Sequence

When the VIN pin voltage rises above 3.6V and the EN pin voltage exceeds the enable threshold of 1.18V, the 5V output LDO enables at once. And the device disables when the VIN pin voltage falls below 3.2V or when the EN pin voltage is below 1.1V. VDD ramp up after 5V LDO works, and also the V3V. Once VDD rise up to 3.8V and V3V is higher than 3V, 4-MOSFETs full bridge allows PWM signal to control for switching. PWM input cannot control full bridge of MOSFETs if VDD drop to 3.36V or V3V drop to 2.7V.

An internal 1.5uA pull up current source to EN pin allows the device enable when EN pin is floating to simply the system design. If an application requires a higher system under voltage lockout threshold, two external resistors divider(R1 and R2) in Figure 9 can be used to achieve an expected system UVLO. The UVLO rising and falling threshold can be calculated by Equation 1 and Equation 2 respectively.

$$V_{rise} = 1.18 \quad (1 + \frac{R1}{R2}) - 1.5uA \quad R1 \qquad (1)$$

$$V_{fall} = 1.1 \quad (1 + \frac{R1}{R2}) - 5.5uA \quad R1 \qquad (2)$$



5V LDO

The SCT63140 has an integrated low-dropout voltage regulator which powered from VIN and supply regulated 5V voltage on VDD pin. The output current capability is 100mA. This LDO can be used to bias the supply voltage of external transmitter controller directly.

It is recommended to connect a decoupling ceramic capacitor of 1uF to 10uF to the VDD pin. Capacitor values outside of the range may cause instability of the internal linear regulator.

Full bridge and PWM Control

The SCT63140 integrate full bridge power stage with only 16mohm on-resistance for each power MOSFET optimized for wireless power transmitter driving the LC resonant circuit. This full bridge is able to operate in a wide switching frequency range from 20KHz to 400KHz for different applications which is completely compatible with WPC's frequency requirement from 100KHz to 205KHz.

PWM1 input controls the half bridge comprised of high side MOSFET Q1 and low side MOSFET Q2, and PWM2 input controls the half bridge comprised of high side MOSFET Q3 and low side MOSFET Q4 as shown in block diagram. The PWM1 and PWM2 independently control the SW1 and SW2 duty cycle and frequency. Logic HIGH will turn off low side FET and turn on high side FET, and logic LOW will turn off high side FET and turn on low side FET.

PWM1 and PWM2 also support tri-state input. When PWM input logic first enters tri-state either from logic HIGH or logic LOW, the states of its controlled FETs stay the same. If the PWM input stays in the tri-state for more than 60ns, its controlled FETs are all turned off, and the corresponding SW output becomes high impedance. The FETs stay off until the PWM logic reaches logic HIGH or logic LOW threshold.

An external 100nF ceramic bootstrap capacitor between BST1 and SW1 pin powers floating high-side power MOSFET Q1's gate driver, and the other 100nF bootstrap capacitor between BST2 and SW2 pin powers for the Q3's. When low side FET is on which means SW is low, the bootstrap capacitor is charged through internal path by VDD power supply rail.

PWM cannot been kept as high level for more than 2ms since the voltage of bootstrap capacitor will be discharged by internal leakage current if high side FET keeps on.

Full Bridge Over Current Protection

The SCT63140 integrates cycle-by-cycle current limit and hiccup mode for over-current protection. The current of the high side FET Q1 and Q3 is sensed and compared to the current limit threshold during each switching cycle. If the current exceeds the threshold, 12.5A typical, the high side FET turns off immediately in present cycle to avoid current increasing even PWM signal is still kept in high level. The over current counter is incremented. If one high side FET occurs over current in 5 consecutive cycles, then all 4 internal FETs are turned off regardless of the PWM inputs. The full bridge enters hiccup mode and will attempt to restart after a time-out period of 24ms typically.

Current Sense

The SCT63140 has a proprietary lossless average current sensing circuit that measures the average input current of full bridge with ±2% accuracy and reports a proportional voltage directly to the ISNS pin. This voltage information on ISNS pin can be send to specialized controller or general MCU for Foreign Object Detection FOD and current demodulation.

When the full bridge of MOSFETs does not work, no current flows to PGND. The DC bias voltage on ISNS pin is 600mV.This DC bias helps set up a suitable voltage bias for the following analog to digital converter in MCU or

3.3V LDO

The SCT63140 has an integrated low-dropout voltage regulator which powered from VDD and supply regulated 3.3V voltage on V3V pin. The output current capability is 100mA. This LDO can be used to bias the supply voltage of MCU directly.

It is recommended to connect a decoupling ceramic capacitor of 1uF to 10uF to the V3V pin. Capacitor values outside of the range may cause instability of the internal linear regulator.

Thermal Shutdown

The SCT63140 protects the device from the damage during excessive heat and power dissipation condition. Once the junction temperature exceeds 155C, the thermal sensing circuit stops two LDOs and full bridge of 4-MOSFETs' working. When the junction temperature falls below 120C, then the device restarts.

Typical Application

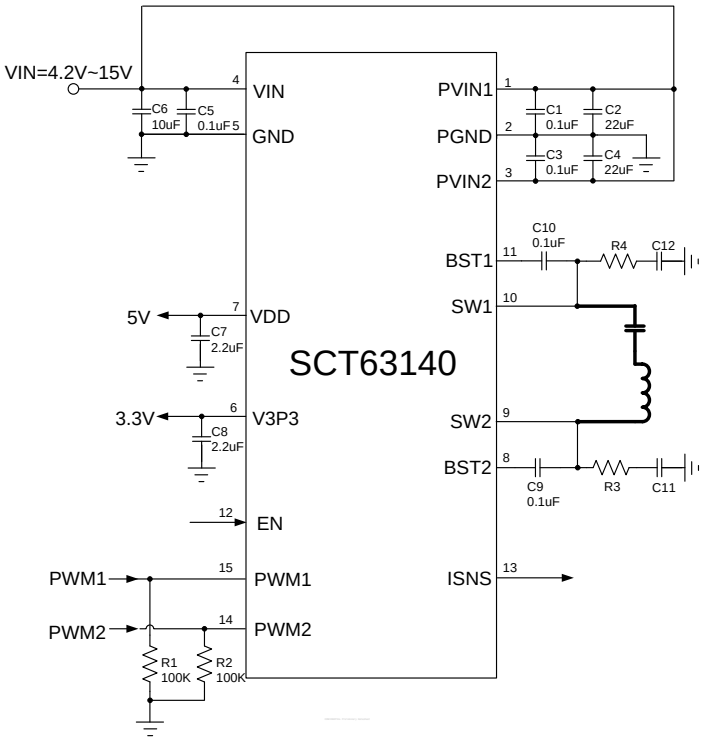


Figure 10. Same Input to VIN and PVIN

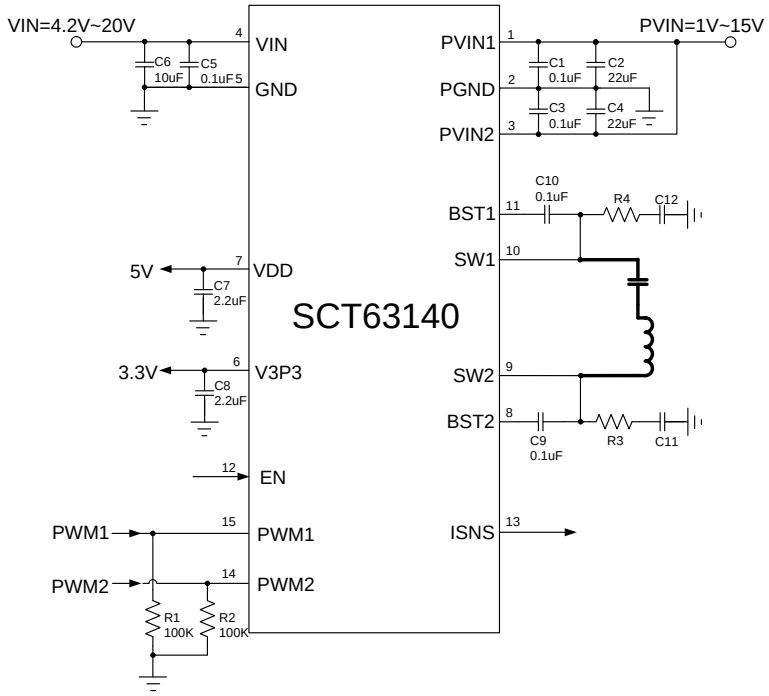


Figure 11. Separate Input to VIN and PVIN

Application Waveforms

F

Figure 12. Power Up

Layout Guideline

Proper PCB layout is a critical for SCT63140 For better results, follow these guidelines as below:

1. Bypass capacitors from PVIN to PGND should put next to PVIN and PGND pin as close as possible especially for the two small capacitors.
2. PGND connect to bottom layer by via between capacitors.
3. Bypass capacitors from VIN to GND should put next to VIN and GND pin as close as possible especially for the small capacitor.
4. Bypass capacitor for VDD place next to VDD pin.
5. Bypass capacitor for V3V place next to V3V pin.

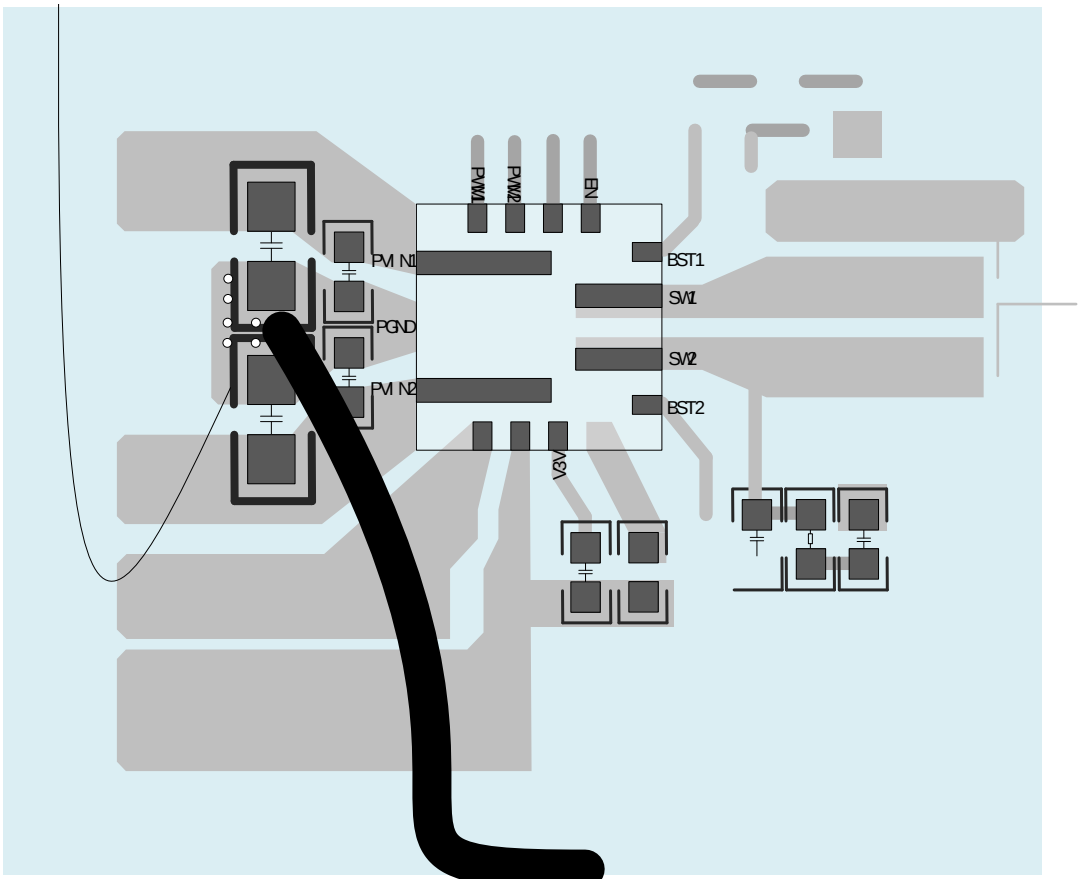
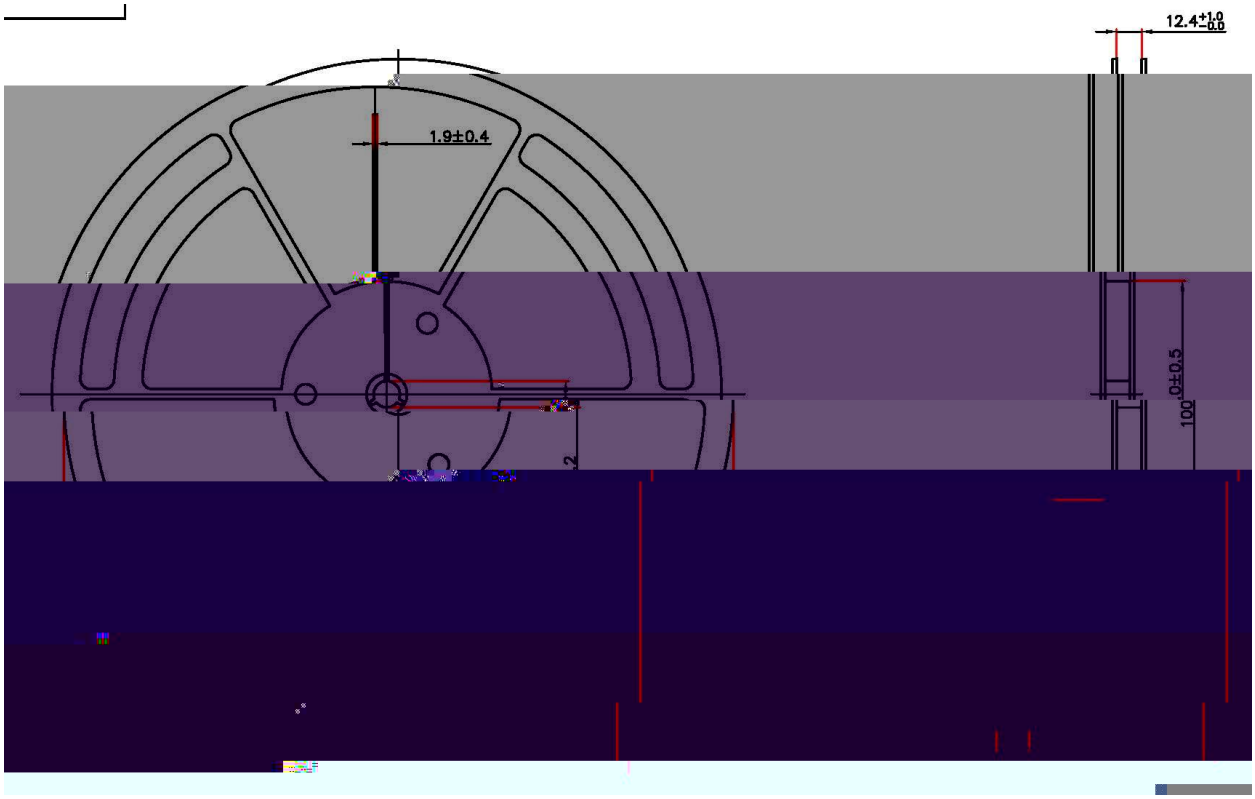


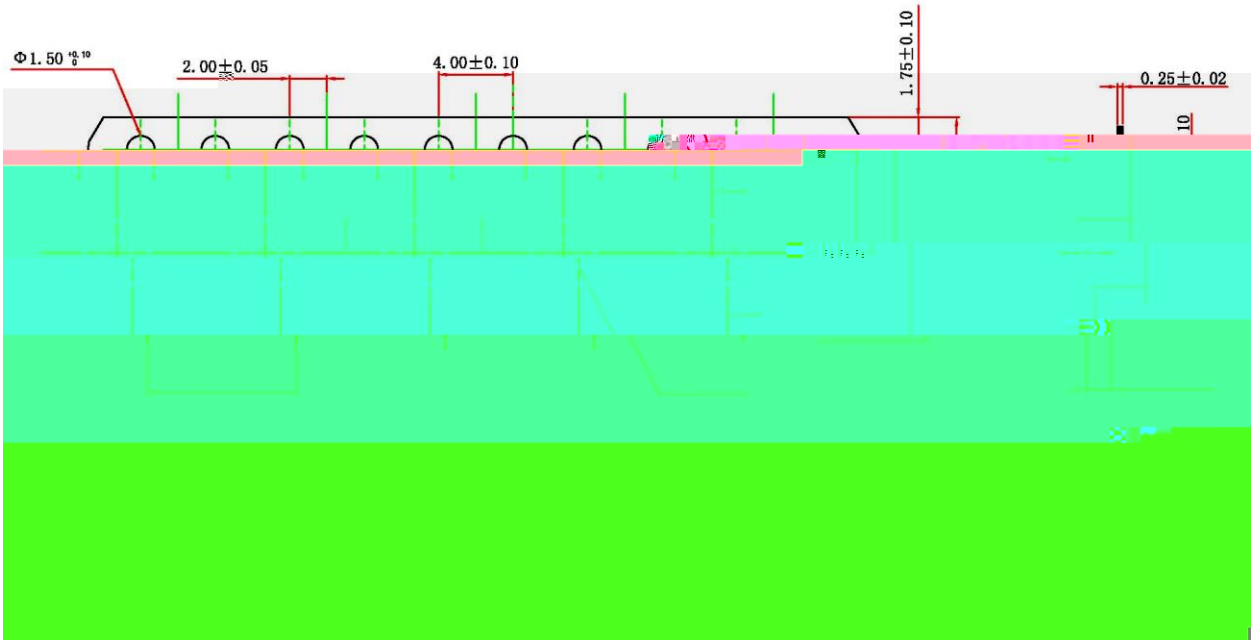
Figure 18. PCB Layout Example

FCQFN-15L (3x3) Package Outline Dimensions

	Symbol	Dimensions in Millimeters		
		Min.	Nom.	Max.
TOTAL THICKNESS	A	0.70	0.75	0.80

Orderable Device	Package Type	Pins	SPQ
SCT63140FMAR	QFN 3mmx3mm	15	5000





PN	DESCRIPTION	COMMENTS
SCT63240	20W High-Integration, High-Efficiency PMIC for Wireless Power Transmitter Integrate a 5V-1A Step-down DC/DC converter compared with SC63140.	• VIN Input Voltage Range: 4.2V-20V • PVIN Input Voltage Range: 1V-17V • Up to 20W Power Transfer • Integrated High Efficiency Full-Bridge Power Stage • Integrated High Efficiency 5V-1A Step-down DC/DC Converter • Optimized for EMI • Build in 3.3V-200mA LDO • Provide 2.5V Voltage Reference • Integrated Input Current sense with ±2% accuracy for FOD and modulation • 3.3V and 5V PWM Signal compatible • Input Under-Voltage Lockout • Over current protection • 3mm*4mm QFN-19L Package

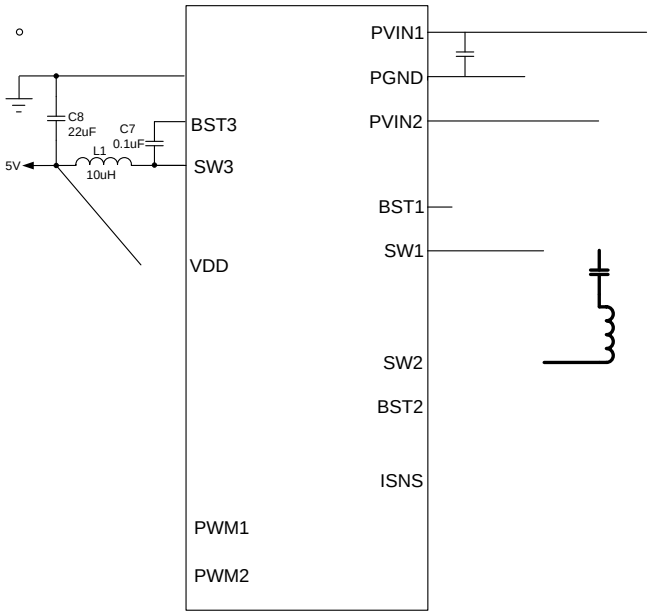


Figure 19. SCT63240 Typical Application

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