SCT242[redacted]

/

&%/ [redacted]

PA[redacted]	TION
[redacted]	

DES[redacted]	
	SW
	GND
	COMP
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8	FB
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(1) [redacted]

(2) 8 [redacted] &*%8

NAME	[redacted]
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	&&

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		88

[redacted]

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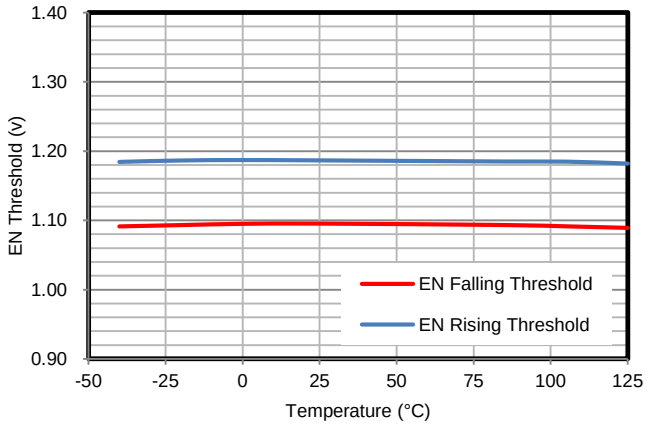
/ 8) &

	.	8 7

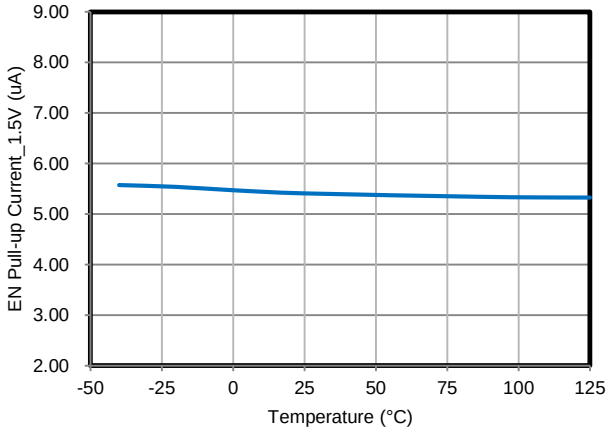
PARAMETER	DEFINITION	MIN	MAX	UNIT
		(-	) %	
		%-	) %	
		) %	& *	8

PARAMETER	DEFINITION	MIN	MAX	UNIT
	[redacted] %&& %&)			
	8 %&) 8 6 8 %%	%*	%*	

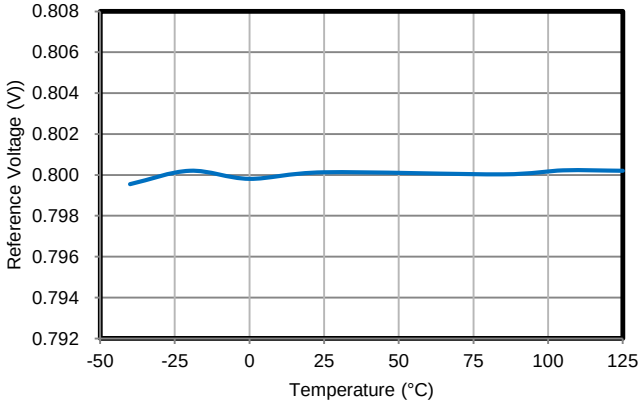
6		61 8 1 6 8 2&	(%%	
8 8	6	72 &%% 8 2&	(%	6
8	6	72		


EN Threshold (v)
1.40
1.30
1.20
1.10
1.00
0.90
-50
-25
0
25
50
75
100
125
Temperature (°C)
EN Falling Threshold
EN Rising Threshold

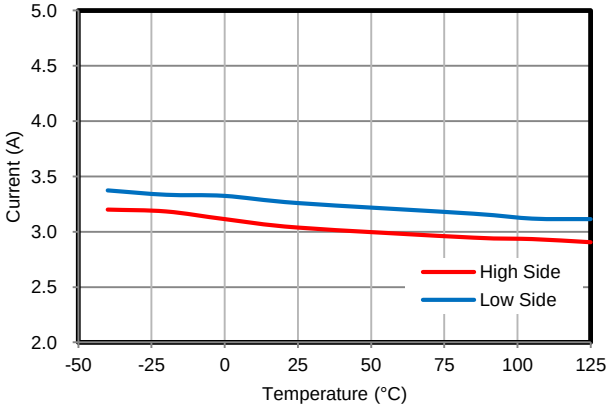
-


EN Pull-up Current_1.5V (uA)
9.00
8.00
7.00
6.00
5.00
4.00
3.00
2.00
-50
-25
0
25
50
75
100
125
Temperature (°C)

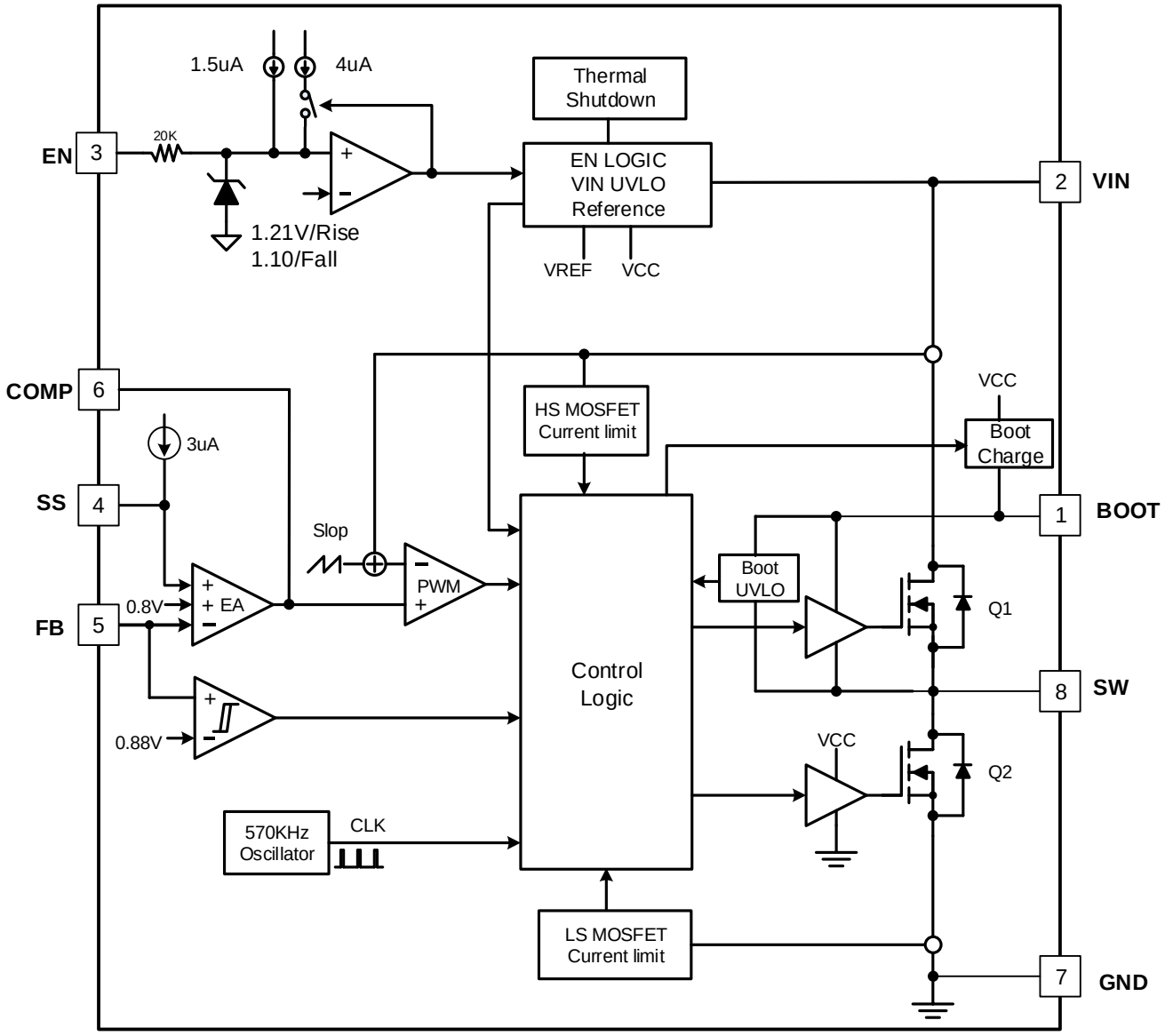
. 8


Reference Voltage (V))
0.808
0.806
0.804
0.802
0.800
0.798
0.796
0.794
0.792
-50
-25
0
25
50
75
100
125
Temperature (°C)

&%


Current (A)
5.0
4.5
4.0
3.5
3.0
2.5
2.0
-50
-25
0
25
50
75
100
125
Temperature (°C)
High Side
Low Side

&& 8


1.5uA
4uA
Thermal
Shutdown
EN
3
20K
EN LOGIC
VIN UVLO
Reference
2
VIN
1.21V/Rise
1.10/Fall
VREF
VCC
COMP
6
HS MOSFET
Current limit
VCC
Boot
Charge
3uA
SS
4
1
BOOT
Slop
PWM
Boot
UVLO
0.8V
+ EA
FB
5
Q1
Control
Logic
8
SW
0.88V
VCC
Q2
570KHz
Oscillator
CLK
LS MOSFET
Current limit
7
GND

& 7

Overview

8) & (-) % 6 &+%
-%

8) &
*, %

* 6

8) & (*) %%

8
8) & +

8) &

Peak Current Mode Control

8) & 6
&
8

8 7 %-
8

*%

8) &
8 8
) %%
7 8
6
&6 8

* 6

Enable and Under Voltage Lockout Threshold

8) & (*
&&-
(&
&& 6 &* 6

Frequency Spread Spectrum

8) &

+ &* &

Bootstrap Voltage Regulator and Low Drop-out Operation

6 7

, (* %

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7 7

, 7)

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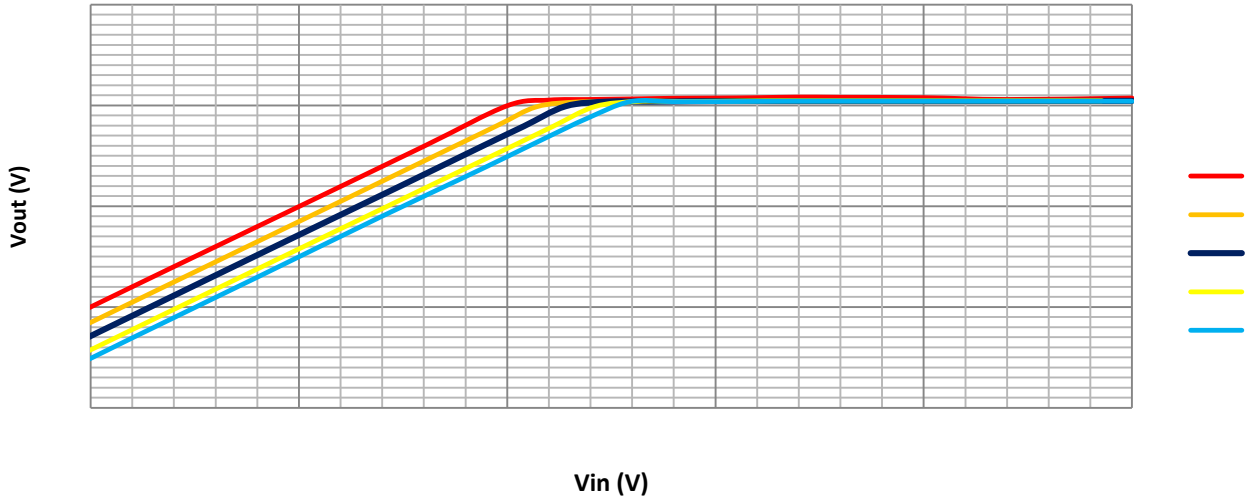
8) &



&) 8 2*

Over Current Limit and Hiccup Mode

& 8) &

7 8
(, 8 * & 6
- & 8

Typical Application

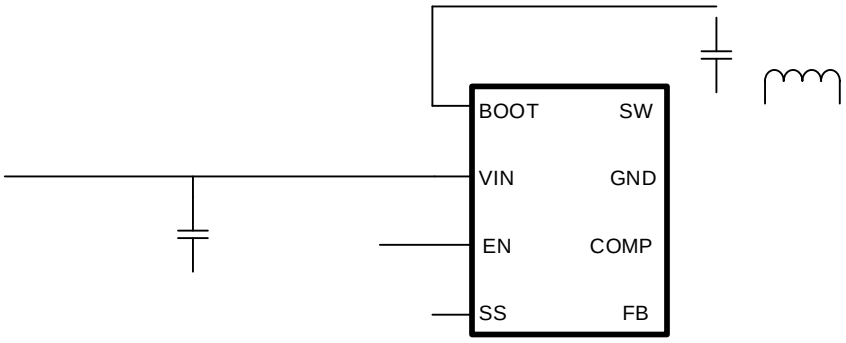


Figure 15. SCT2421 Design Example, 3.3V Output with Programmable UVLO

Design Parameters

Design Parameters	Example Value
	) (-) %
	((
8	6
	*, %
	&+ *
	*, +
	) ++

Output Voltage

* +
+ &%
* *

*
/
•
%-

Table 1. R_5, R_6 Value for Common Output Voltage (Room Temperature)

V_{OUT}	R_5	R_6
& -	& ,	&%
*	& *	&%
((	(& +	&%
*	* (+	&%
&	&) (	&%
)	.)	&%

Under Voltage Lock-Out

6 &
&*

* , 6
) +) + , &, ( ) &

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- 8
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+ +

6

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&%

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- 8
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(6

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2 /

&(

8

&) *%

&)

), , *% 6 %&

Bootstrap Capacitor Selection

6 %& 7 6
* &%

Output Capacitor Selection

&*

&*

-
-
-
- 8
-
-

8 8

),

Compensation Components

8) & 6
) 8, 8+ 8
&+

_____ *

8+

(8+

+

_____ +

Table 2: Compensation Values for Typical Ceramic and Polymer Output Capacitors

Inverting Power application

8) &

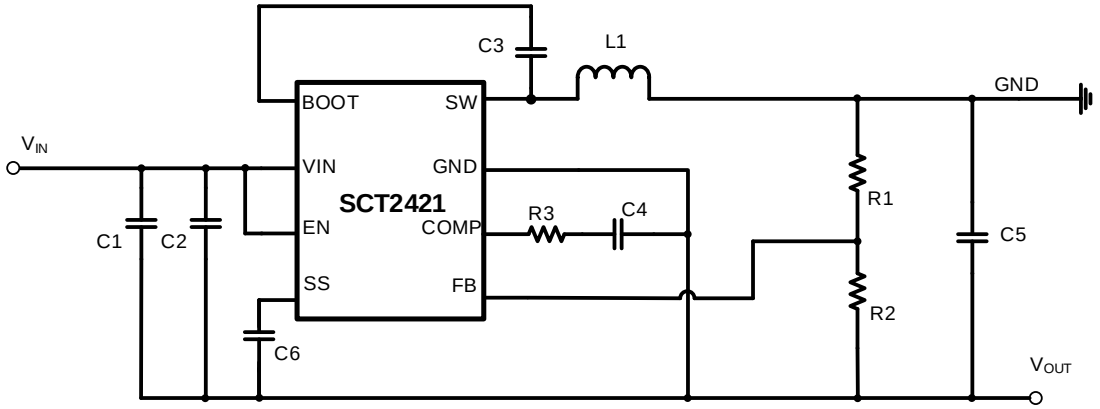
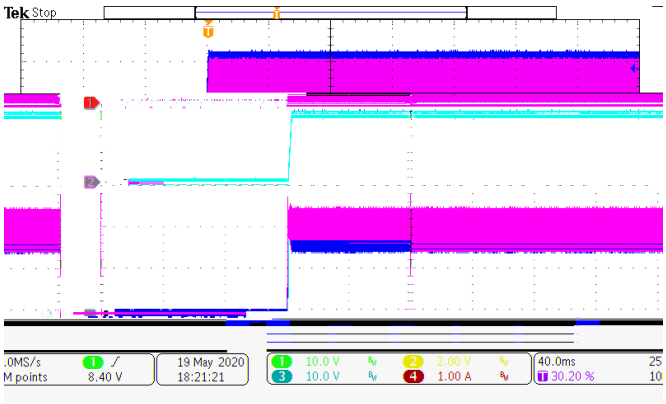


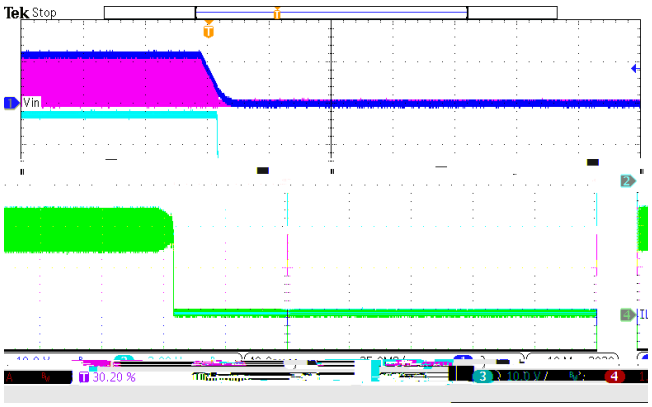
Figure 16. SCT2421 Inverting Power Supply

Application Waveforms

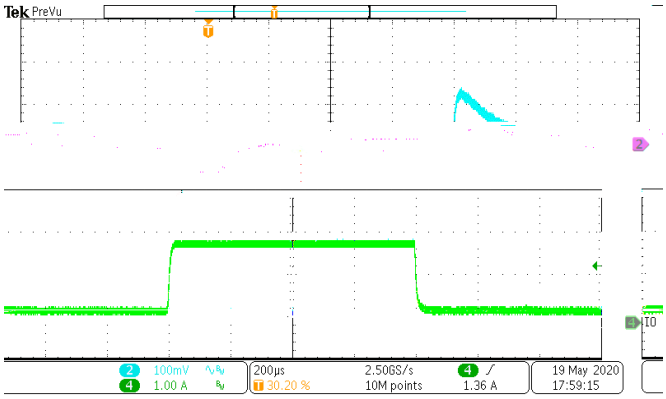
2& 2((2 6



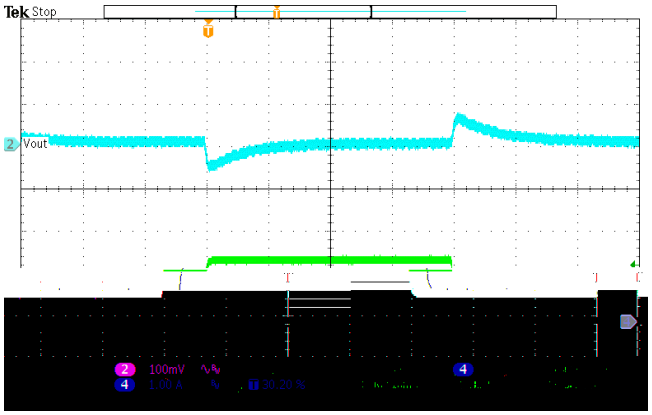
&



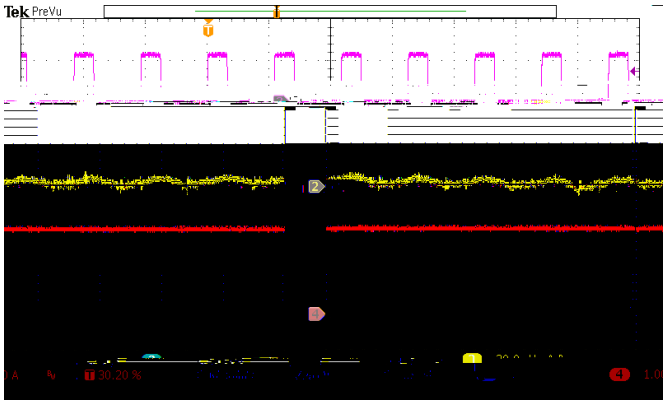
&



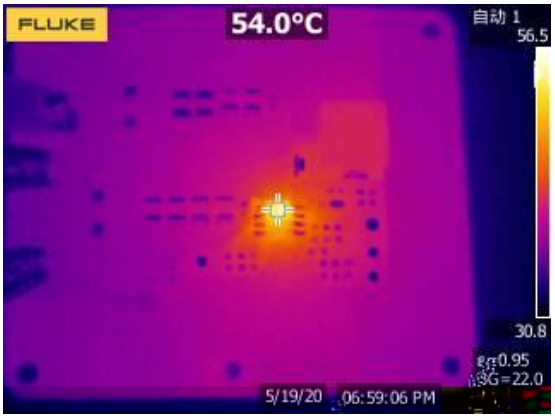
& % 6 &-6 &+6



% %+6 &)6 &+6



& 2 6



((6

Layout Guideline

87 8) &

/

1.

87

2.

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87 8

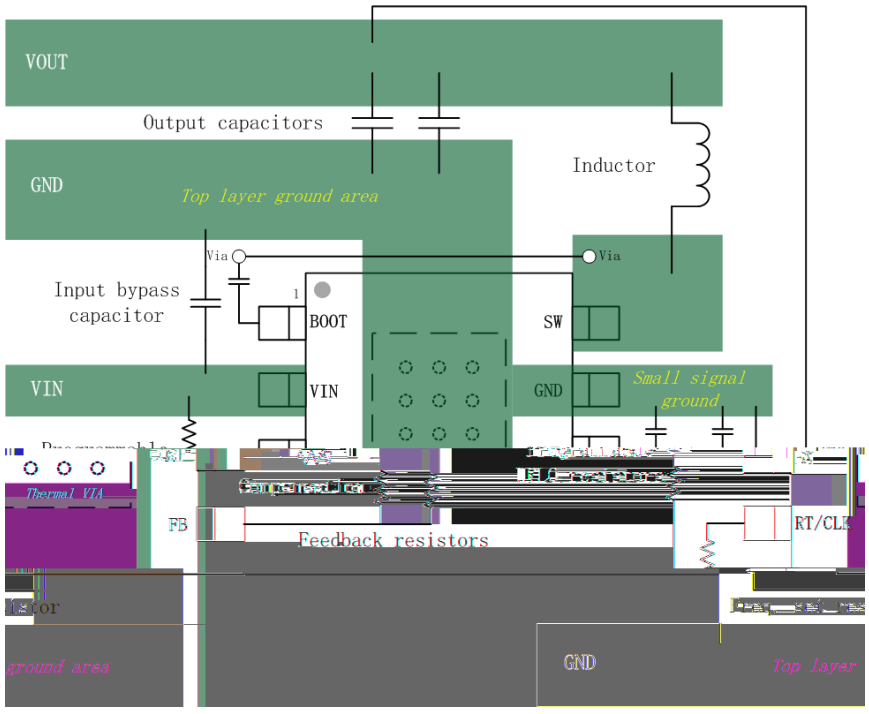
5. 87

6. 8 8

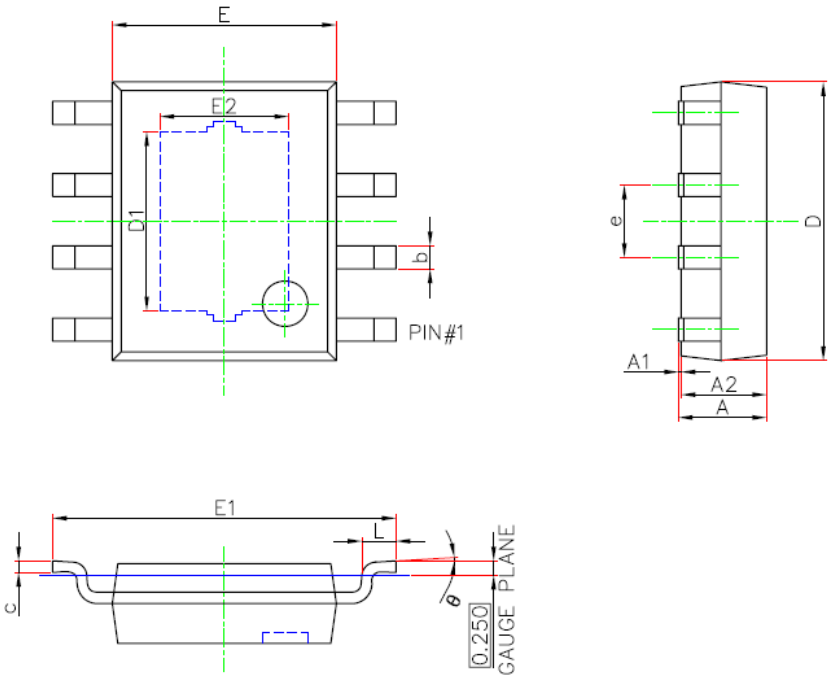
7.

8. 7

9.



+ 87



- . * &(%

6	&(%%	&, %%	%%* &	%%+,
6 &	%%%%	%&%%	%%%%	%%%)
6	&(* %	&* * %	%%* (	%%+ &
	%((%	%* &%	%%&(	%% %
	%&, %	% * %	%%%)	%%&%
	) , %%	* &%%	%&- *	% %&
&	(%* %	(* %	%& %	%& -
	(- %%	) %%%	%&* %	%&*,
&	* - %%	+ %%	% -	%))
	&+%	(+%	%% *	%% (
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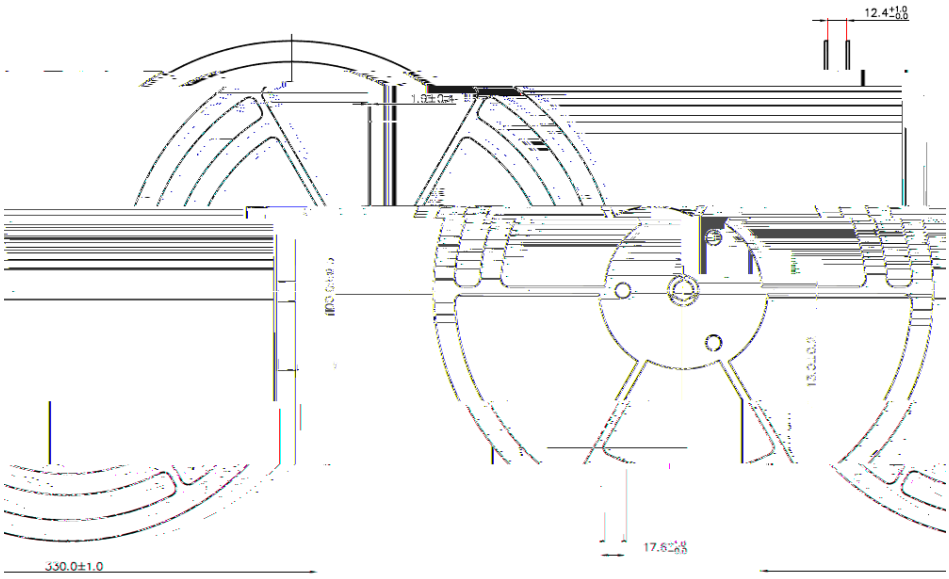
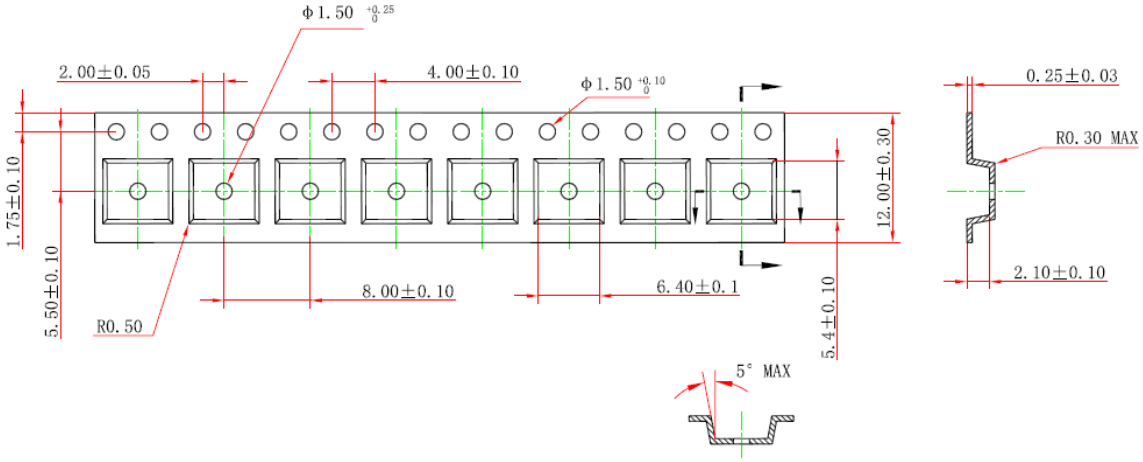
	%) %%	& , %	%%&+	%%* %
θ	%	-	%	-

NOTE:

1. 8 %
2.
3. 6
4.
5.
6. 8 87


12.4+1.0 -0.0
330.0±1.0


Φ1.50 +0.25 0
2.00±0.05
4.00±0.10
Φ1.50 +0.10 0
1.75±0.10
5.50±0.10
R0.50
8.00±0.10
6.40±0.1
12.00±0.30
5.4±0.10
5° MAX
0.25±0.03
R0.30 MAX
2.10±0.10