

- EMI Reduction with Switching Node Ringing-free
- 400kHz Switching Frequency with 6% Frequency Spread Spectrum FSS
- Pulse Skipping Mode PSM with 20uA Quiescent Current in Light Load Condition
- 3.8V-28V Wide Input Voltage Range
- 0.8V \pm 1% Feedback Reference Voltage
- Fully Integrated 85m Ω R_{dson} High Side MOSFET and 58m Ω R_{dson} Low Side MOSFET
- 1uA Shut-down Current
- 80ns Minimum On-time
- Precision Enable Threshold for Programmable UVLO Threshold and Hysteresis
- Low Dropout Mode Operation
- 4ms Built-in Soft Start Time
- Output Over Voltage Protection
- Thermal Shutdown Protection at 160°C
- Available in ESOP-8 Package

The SCT9336 is 5A synchronous buck converters with up to 28V wide input voltage range, which fully integrates an 85m Ω high-side MOSFET and a 58m Ω low-side MOSFET to provide high efficiency step-down DCDC conversion. The SCT9336 adopts peak current mode control with the integrated compensation network, which makes SCT9336 easily to be used by minimizing the off-chip component count. The SCT9336 supports the Pulse Skipping Modulation (PSM) with typical 20uA Ultra-Low Quiescent.

The SCT9336 is an Electromagnetic Interference (EMI) friendly buck converter with implementing optimized design for EMI reduction. The SCT9336 features Frequency Spread Spectrum FSS with \pm 6% jittering span of the 400kHz switching frequency and modulation rate 1/512 of switching frequency to reduce the conducted EMI. The converter has proprietary designed gate driver scheme to resist switching node ringing without sacrificing MOSFET turn-on and turn-off time

- White Goods, Home Appliance
- Surveillance
- Audio, WiFi Speaker
- Printer, Charging Station
- DTV, STB, Monitor/LCD Display

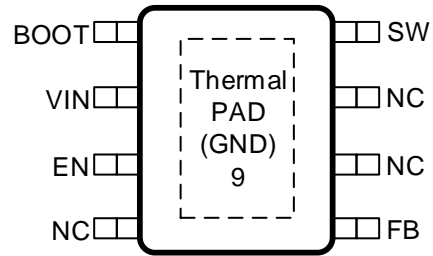
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision 1.0: Release to Market

PART NUMBER	PACKAGE MARKING	PACKAGE DISCRIPTION
SCT9336STE	9336	8-Lead Plastic ESOP
1 For Tape & Reel, Add Suffix R (e.g. SCT9336STER).		

Over operating free-air temperature unless otherwise noted⁽¹⁾

DESCRIPTION	MIN	MAX	UNIT
BST	-0.3	40	V
VIN, SW, EN	-0.3	34	V
BST-SW	-0.3	6	V
FB	-0.3	5.5	V
Operating junction temperature ⁽²⁾	-40	125	C
Storage temperature T _{STG}	-65	150	C



8-Lead Plastic E-SOP

- (1) Stresses beyond those listed under Absolute Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.
- (2) The IC includes over temperature protection to protect the device during overload conditions. Junction temperature will exceed 150°C when over temperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime.

NAME **NO.** **PIN** **operation"** **era**

SW	8	Switching node of the buck converter.
Thermal Pad	9	GND and Heat dissipation path of die. Must be connected to ground plane on PCB for proper operation and optimized thermal performance.

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V _{IN}	Input voltage range	3.8	28	V
T _J	Operating junction temperature	-40	125	°C

PARAMETER	DEFINITION	MIN	MAX	UNIT
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V_{ESK} Dq□%

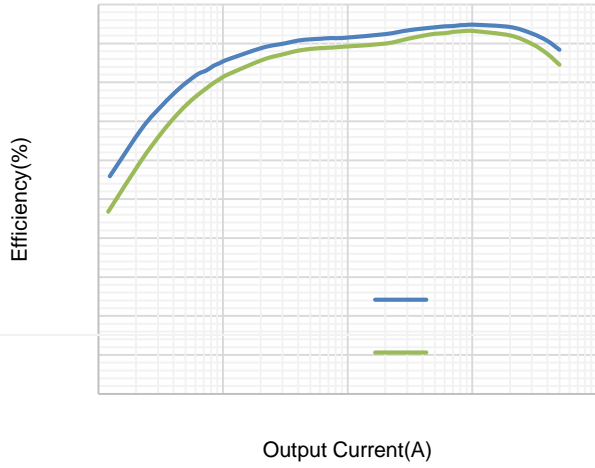


Figure 1. Efficiency vs Load Current, Vin=12V



Figure 2. Efficiency vs Load Current, Vin=24V

Figure 3. Shut-down Current vs Temperature

Figure 4. Quiescent Current vs Temperature

Figure 5. Reference Voltage vs Temperature

Figure 6. VIN UVLO vs Temperature

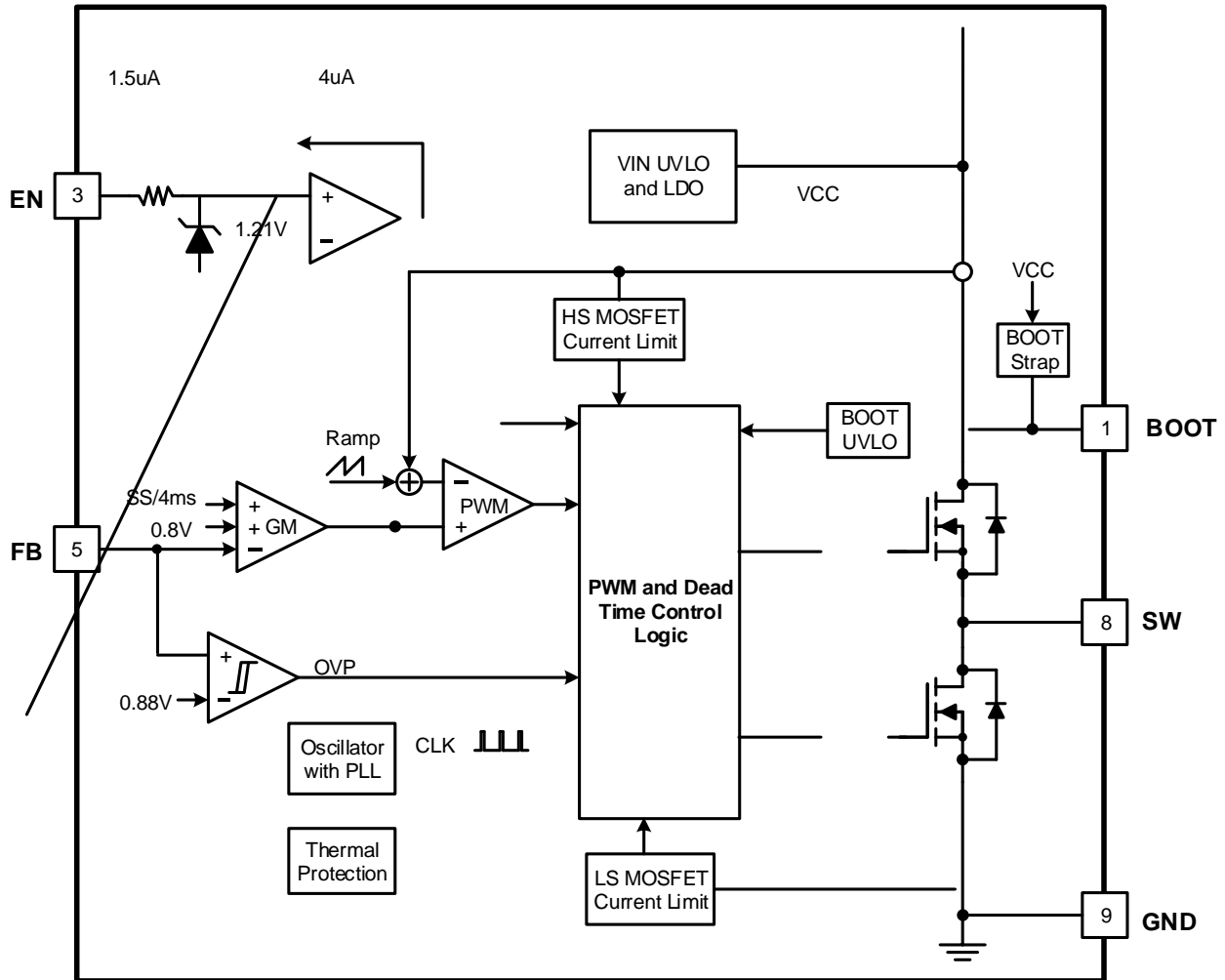


Figure 7. Functional Block Diagram

Overview

The SCT9336 device is 3.8V-28V input, 5A output, EMI friendly, fully integrated synchronous buck converters. The

An internal 1.5uA pull up current source connected from internal LDO power rail to EN pin guarantees that floating EN pin automatically enables the device. For the application requiring higher VIN UVLO voltage than the default setup, there is a 4uA hysteresis pull up current source on EN pin which configures the VIN UVLO voltage with an off-chip resistor divider R3 and R4, shown in Figure 8. The resistor divider R3 and R4 are calculated by equation (1) and (2).

EN pin is a high voltage pin and can be directly connected to VIN to automatically start up the device with VIN rising to its internal UVLO threshold.

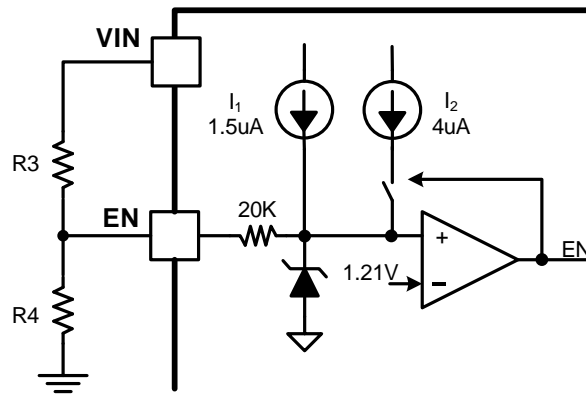


Figure 8. Adjustable VIN UVLO

$$\frac{V_{ENR} - V_{EMF}}{I_2 - I_1} = \frac{R_3}{R_4} \tag{1}$$

$$V_{ENR} = V_{EMF} + \frac{I_2 - I_1}{I_1} \cdot V_{EMF} \tag{2}$$

Where:

- Vstart: Vin rise threshold to enable the device
- Vstop: Vin fall threshold to disable the device
- I₁=1.5uA
- I₂=4uA
- V_{ENR}=1.18V
- V_{EMF}=1.1V

EMI Reduction with Frequency Spread Spectrum and Switching Node Ringing-free

In some applications, the system EMI test must meet EMI standards EN55011 and EN55022. To improve EMI performance, SCT9336 adopts Frequency Spread Spectrum (FSS) to spread the switching noise over a wider band and therefore reduces conducted and radiated interference peak amplitude at particular frequency. The SCT9336 features 400kHz switching frequency with spreading frequency of +/-6% and modulation rate 1/512 of switching frequency. The FSS technique effectively decreases the EMI noise by spreading the switching frequency from fixed 400kHz to a range 517kHz ~ 583kHz. As a result, the harmonic wave amplitude is reduced and the harmonic wave band is wider.

In buck converter, the switching node ringing amplitude and cycles are critical especially related to the high frequency radiation EMI noise. The SCT9336 implements the multi-level gate driver speed technique to achieve the

switching node ringing-free without sacrificing the switching node rise/fall slew rate and power efficiency of the converter. The switching node ringing amplitude and cycles are damped by the built-in MOSFETs gate driving technique (SCT Patented Proprietary Design).

Over Current Protection

The SCT9336 implements over current protection with cycle-by-cycle limiting high-side MOSFET peak current and low-side MOSFET valley current to avoid inductor current running away during unexpected overload or output hard short condition. The inductor current I_L is monitored during high-side MOSFET Q1 and low-side MOSFET Q2 on.

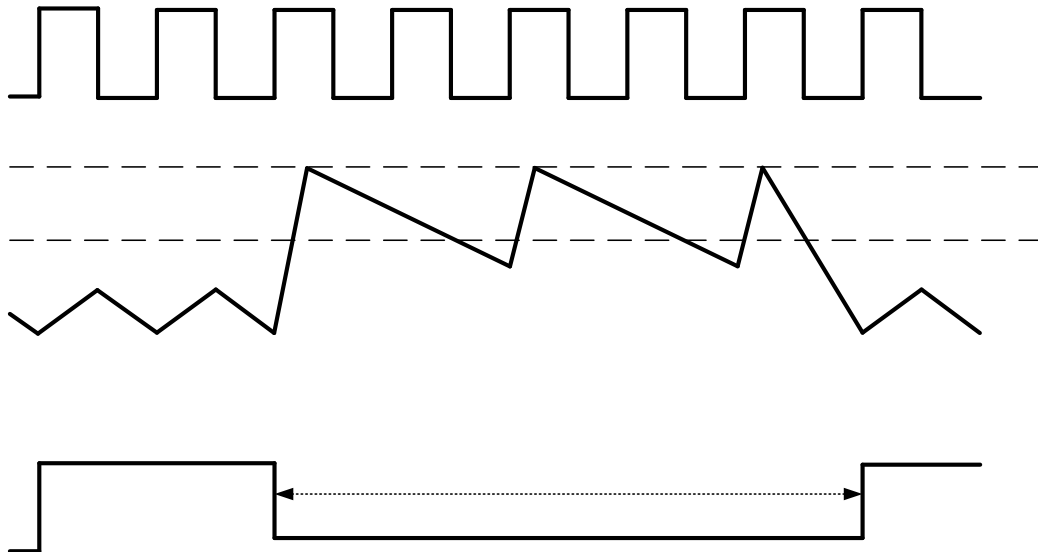


Figure 9. Over Current Protection

When overload or hard short happens, once the high-side MOSFET Q1 current exceeds the HS limit, Q1 is turned off immediately and Q2 is turned on till the low-side MOSFET Q2 current goes beneath the LS limit and next clock rising-edge comes. Then, Q1 is turned on and Q2 is turned off in another Over protection cycle until the overload or hard short is released

Over Voltage Protection and Minimum On-time

Both SCT9336 features buck converter output over voltage protection (OVP). If the output feedback pin voltage exceeds 110% of feedback reference voltage (0.8V), the converter stops switching immediately. When the output feedback pin voltage drops below 105% of feedback reference voltage, the converter resumes to switching. The OVP function prevents the connected output circuitry damaged from un-predictive overvoltage. Featured feedback overvoltage protection also prevents dynamic voltage spike to damage the circuitry at load during fast loading transient.

The high-side MOSFET Q1 has minimum on-time 80ns typical limitation. While the device operates at minimum on-time, further increasing V_{IN} results in pushing output voltage beyond regulation point. With output feedback over voltage protection, the converter skips pulse by turning off high-side MOSFET Q1 and prevents output running away higher to damage the load.

PSM Working Modes

In heavy load condition, the SCT9336 forces the device operating at forced Pulse Width Modulation (PWM) mode. When the load current decreasing, the internal COMP net voltage decreases as the inductor current down. With the load current further decreasing, the COMP net voltage decreases and be clamped at a voltage corresponding to the 600mA peak inductor current. When the load current approaches zero, the SCT9336 enter Pulse Skipping Mode (PSM) mode to increase the converter power efficiency at light load condition. When the inductor current decreases

to zero, zero-cross detection circuitry on high-side MOSFET Q1 forces the Q1 off till the beginning of the next switching cycle. The buck converter does not sink current from the load when the output load is light and converter works in PSM mode.

Bootstrap Voltage Regulator

An external bootstrap capacitor between BST and SW pin powers floating high-side power MOSFET gate driver. The bootstrap capacitor voltage is charged from an integrated voltage regulator when high-side power MOSFET is off and low-side power MOSFET is on.

The floating supply (BST to SW) UVLO threshold is 2.7V rising and hysteresis of 350mV. When the converter operates with high duty cycle or prolongs in sleep mode for certain long time, the required time interval to recharging bootstrap capacitor is too long to keep the voltage at bootstrap capacitor sufficient. When the voltage across bootstrap capacitor drops below 2.35V, BST UVLO occurs. The SCT9336 intervenes to turn on low side MOSFET periodically to refresh the voltage of bootstrap capacitor to guarantee operation over a wide duty range.

Low Drop-out Regulation

To support the application of small voltage-difference between V_{out} and V_{in} , the Low Drop Out (LDO) Operation is implemented by the SCT9336. The Low Drop Out Operation is triggered automatic when the off time of the high-side power MOSFET exceeds the minimum off time limitation.

In low drop out operation, high-side MOSFET remains ON as long as the BST pin to SW pin voltage is higher than BST UVLO threshold. When the voltage from BST to SW drops below 2.35V, the high-side MOSFET turns off and low-side MOSFET turns on to recharge bootstrap capacitor periodically in the following several switching cycles. Only 100ns of low side MOSFET turning on in each refresh cycle minimizes the output voltage ripple. Low-side MOSFET may turn on for several times till bootstrap voltage is charged to higher than 2.7V for high-side

MOSFET working normally. Then high-side MOSFET turns on and remains on until bootstrap voltage drops to trigger bootstrap UVLO again. Thus, the effective duty cycle of the switching regulator during Low Drop-out LDO operation can be very high even approaching 100% as shown in Figure 10.

During ultra-low voltage difference of input and output voltages, i.e. the input voltage ramping down to power down, the output can track input closely thanks to LDO operation mode.

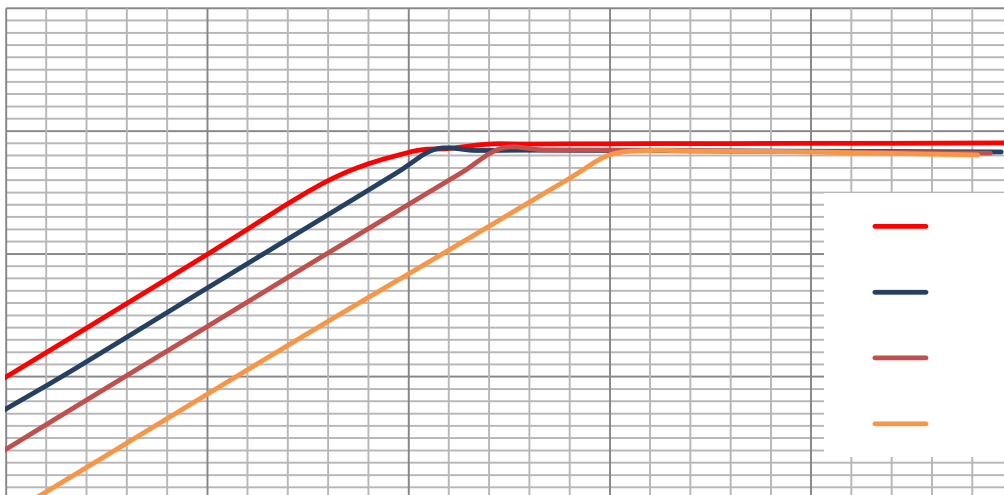
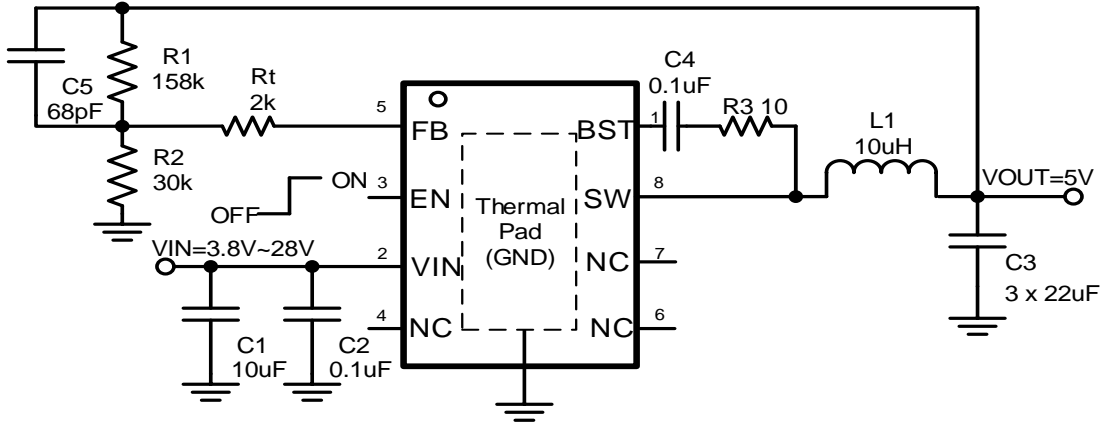


Figure 10. SCT9336 LDO Mode Waveform

Thermal Shutdown

Once the junction temperature in the SCT9336 exceeds 160°C, the thermal sensing circuit stops converter switching and restarts with the junction temperature falling below 125°C. Thermal shutdown prevents the damage on device during excessive heat and power dissipation condition.

Typical Application



*For input voltage higher than 18V, R3=10 is highly recommend.
Figure 11. 24V Input, 5V/3A Output

Design Parameters

Design Parameters	Example Value
Input Voltage	24V
Output Voltage	5V
Output Current	3A
Output voltage ripple (peak to peak)	±0.3V
Switching Frequency	400kHz

Input Capacitor Selection

For good input voltage filtering, choose low-ESR ceramic capacitors. A ceramic capacitor 10 μ F is recommended for the decoupling capacitor and a 0.1 μ F ceramic bypass capacitor is recommended to be placed as close as possible to the VIN pin of the SCT9336.

Use Equation (3) to calculate the input voltage ripple:

(3)

Where:

- C_{IN} is the input capacitor value
- f_{sw} is the converter switching frequency
- I_{OUT} is the maximum load current

Due to the inductor current ripple, the input voltage changes if there is parasitic inductance and resistance between the power supply and the VIN pin. It is recommended to have enough input capacitance to make the input voltage ripple less than 100mV. Generally, a 35V/10uF input ceramic capacitor is recommended for most of applications. Choose the right capacitor value carefully with considering high-capacitance ceramic capacitors DC bias effect, which has a strong influence on the final effective capacitance.

Inductor Selection

The performance of inductor affects the power supply's steady state operation, transient behavior, loop stability, and buck converter efficiency. The inductor value, DC resistance (DCR), and saturation current influences both efficiency and the magnitude of the output voltage ripple. Larger inductance value reduces inductor current ripple and therefore leads to lower output voltage ripple. For a fixed DCR, a larger value inductor yields higher efficiency via reduced RMS and core losses. However, a larger inductor within a given inductor family will generally have a greater series resistance, thereby counteracting this efficiency advantage.

Inductor values can have $\pm 20\%$ or even $\pm 30\%$ tolerance with no current bias. When the inductor current approaches saturation level, its inductance can decrease 20% to 35% from the value at 0-A current depending on how the inductor vendor defines saturation. When selecting an inductor, choose its rated current especially the saturation current larger than its peak current during the operation.

To calculate the current in the worst case, use the maximum input voltage, minimum output voltage, maximum load current and minimum switching frequency of the application, while considering the inductance with -30% tolerance and low-power conversion efficiency.

For a buck converter, calculate the inductor minimum value as shown in equation (4).

(4)

Where:

- K_{IND} is the coefficient of inductor ripple current relative to the maximum output current.

Therefore, the peak switching current of inductor, I_{LPEAK} , is calculated as in equation (5).

(5)

Set the current limit of the SCT9336 higher than the peak current I_{LPEAK} and select the inductor with the saturation current higher than the current limit. The inductor's DC resistance (DCR) and the core loss significantly affect the efficiency of power conversion. Core loss is related to the core material and different inductors have different core

loss. For a certain inductor, larger current ripple generates higher DCR and ESR conduction losses and higher core loss.

Output Capacitor Selection

For buck converter, the output capacitor value determines the regulator pole, the output voltage ripple, and how the regulator responds to a large change in load current. The output capacitance needs to be selected based on the most stringent of these three criteria.

For small output voltage ripple, choose a low-ESR output capacitor like a ceramic capacitor, for example, X5R and X7R family. Typically, 1~3x 22μF ceramic output capacitors work for most applications. Higher capacitor values can be used to improve the load transient response. Due to a capacitor’s de-rating under DC bias, the bias can significantly reduce capacitance. Ceramic capacitors can lose most of their capacitance at rated voltage. Therefore, leave margin on the voltage rating to ensure adequate effective capacitance.

From the required output voltage ripple, use the equation (6) to calculate the minimum required effective capacitance, C_{OUT}.

$$\text{-----} \tag{6}$$

Where

- V_{OUTRipple} is output voltage ripple caused by charging and discharging of the output capacitor.
- ΔI_{LPP} is the inductor peak to peak ripple current, equal to k_{IND} * I_{OUT}.
- f_{SW} is the converter switching frequency.

The allowed maximum ESR of the output capacitor is calculated by the equation (7).

$$\text{-----} \tag{7}$$

The output capacitor affects the crossover frequency f_c. Considering the loop stability and effect of the internal loop compensation parameters, choose the crossover frequency less than 55 kHz (—) without considering the feed-forward capacitor. A simple estimation for the crossover frequency without feed forward capacitor is shown in equation (8), assuming C_{OUT} has small ESR.

$$\text{-----} \tag{8}$$

Where

- G_M is the transfer conductance of the error amplifier (300uS).
- G_{MP} is the gain from internal COMP to inductor current, which is 5A/V.
- f_c is the cross over frequency.

Additional capacitance de-rating for aging, temperature and DC bias should be factored in which increases this minimum value. Capacitors generally have limits to the amount of ripple current they can handle without failing or producing excess heat. An output capacitor that can support the inductor ripple current must be specified. The capacitor data sheets specify the RMS (Root Mean Square) value of the maximum ripple current. Equation (9) can be used to calculate the RMS ripple current the output capacitor needs to support.

$$\text{-----} \tag{9}$$

Output Feed-Forward Capacitor Selection

The SCT9336 has the internal integrated loop compensation as shown in the function block diagram. The compensation network includes a 18k resistor and a 7.6nF capacitor. Usually, the type II compensation network has a phase margin between 60 and 90 degree. However, if the output capacitor has ultra-low ESR, the converter results in low phase margin. To increase the converter phase margin, a feed-forward cap C_{ff} is used to boost the phase margin at the converter cross-over frequency f_c . Equation (10) is used to calculate the feed-forward capacitor.

$$\text{-----} \tag{10}$$

Output Feedback Resistor Divider Selection

The SCT9336 features external programmable output voltage by using a resistor divider $n = M \text{ funcdiv_c}$ a phase

Application Waveforms

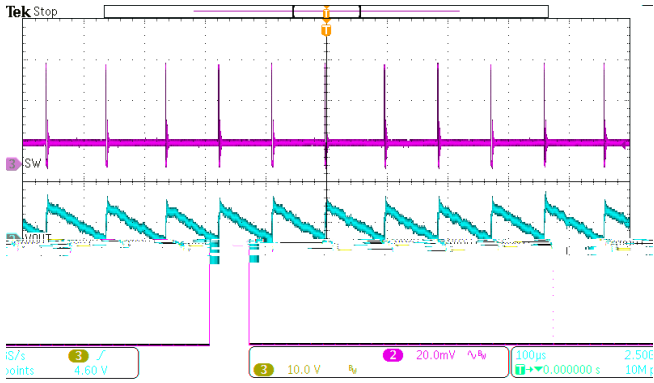


Figure 12. SW node waveform and Output Ripple
VIN=24V, IOUT=10mA

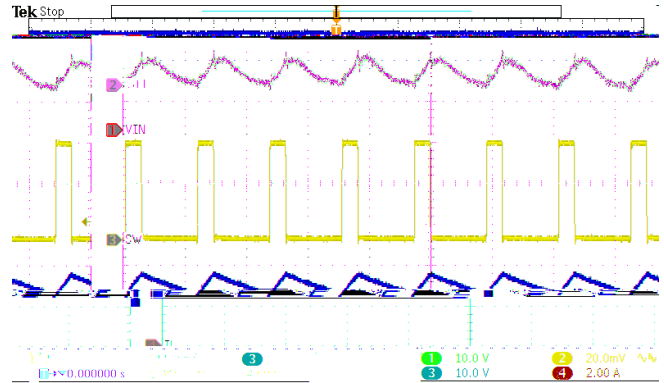


Figure 13. SW node waveform and Output Ripple
VIN=24V, IOUT=3A

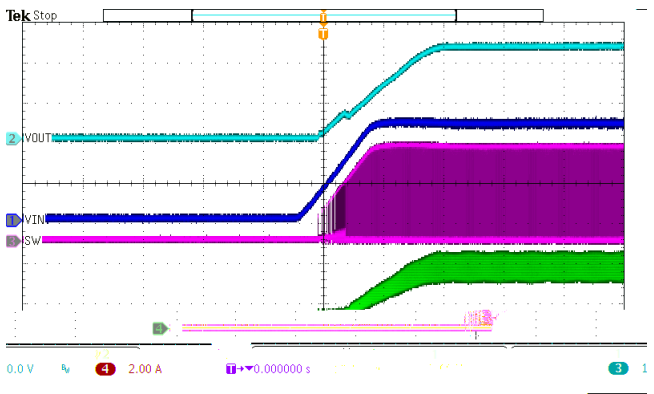


Figure 14. Power Up
VIN=24V, VOUT=5V, IOUT=3A

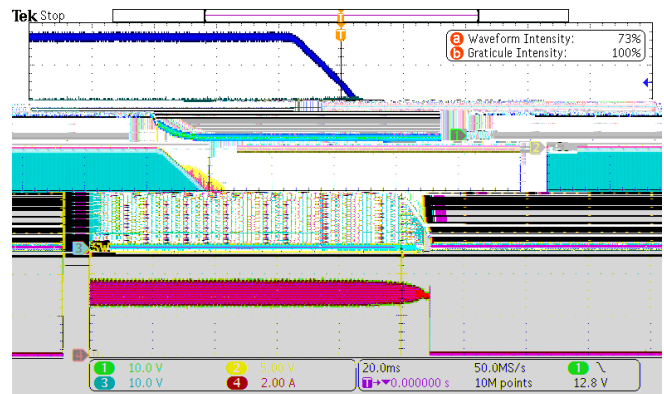


Figure 15. Power Down
VIN=24V, VOUT=5V, IOUT=3A

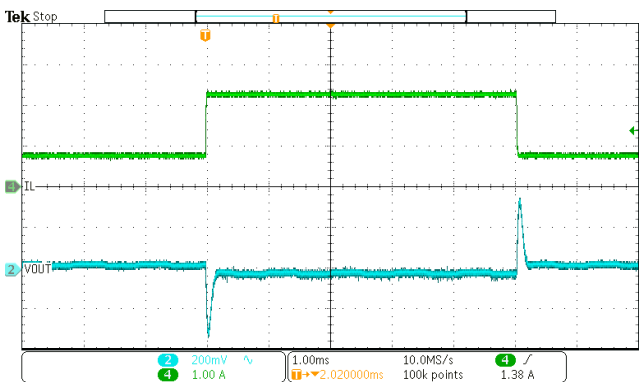


Figure 16. Load Transient
VOUT=5V, IOUT=0.75A to 2.25 A, SR=250mA/us

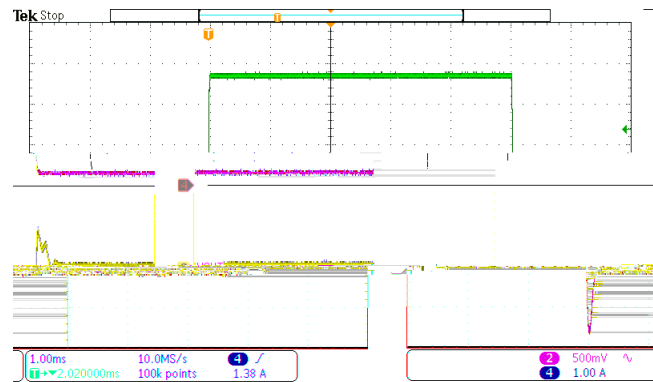


Figure 17. Load Transient
VOUT=5V, IOUT=0.3A to 2.7A, SR=250mA/us

Layout Guideline

The regulator could suffer from instability and noise problems without carefully layout of PCB. Radiation of high-frequency noise induces EMI, so proper layout of the high-frequency switching path is essential. Minimize the length and area of all traces connected to the SW pin, and always use a ground plane under the switching regulator to minimize coupling. The input capacitor needs to be very close to the VIN pin and GND pin to reduce the input supply ripple. Place the capacitor as close to VIN pin as possible to reduce high frequency ringing voltage on SW pin as well. Figure 18 is the recommended PCB layout of SCT9336.

The layout needs be done with well consideration of the thermal. A large top layer ground plate using multiple thermal vias is used to improve the thermal dissipation. The bottom layer is a large ground plane connected to the top layer ground by vias.

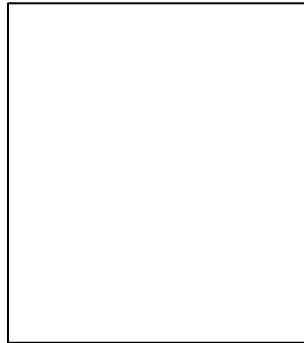


Figure 18. PCB Layout Example

Thermal Considerations

The maximum IC junction temperature should be restricted to 125°C under normal operating conditions. Calculate the maximum allowable dissipation, $P_{D(max)}$, and keep the actual power dissipation less than or equal to $P_{D(max)}$. The maximum-power-dissipation limit is determined using Equation (12).

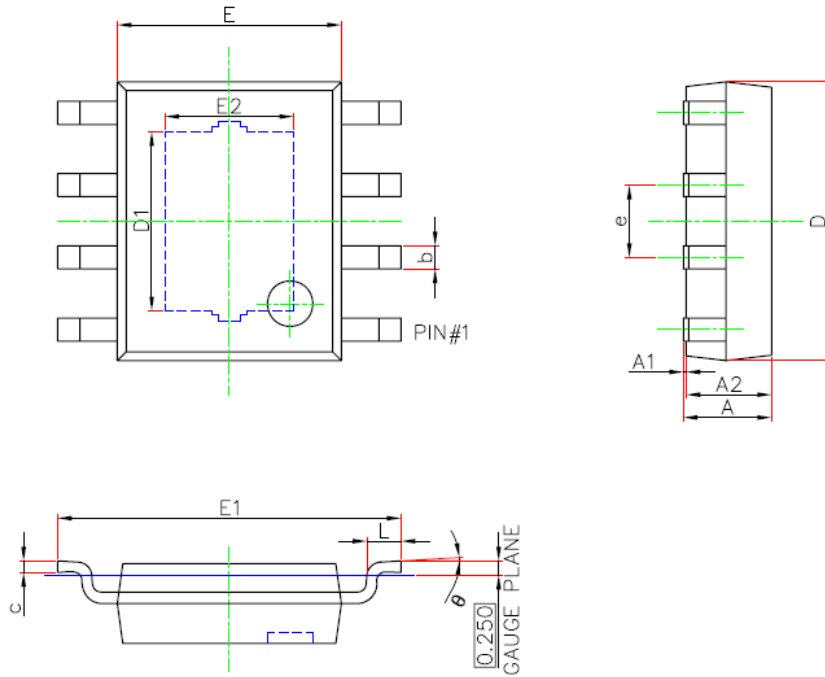
$$\text{_____} \quad (12)$$

where

- T_A is the maximum ambient temperature for the application.

- $R_{\theta JA}$ is the junction-to-ambient thermal resistance given in the Thermal Information table.

The real junction-to-ambient thermal resistance $R_{\theta JA}$ of the package greatly depends on the PCB type, layout, thermal pad connection and environmental factor. Using thick PCB copper and soldering the GND to a large ground plate enhance the thermal performance. Using more vias connects the ground plate on the top layer and bottom layer around the IC without solder mask also enhance the thermal capability.

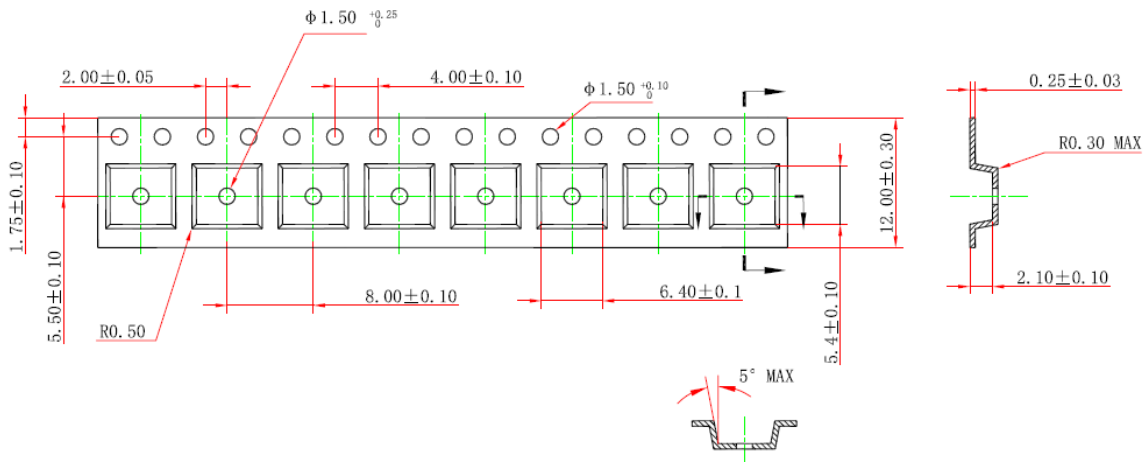
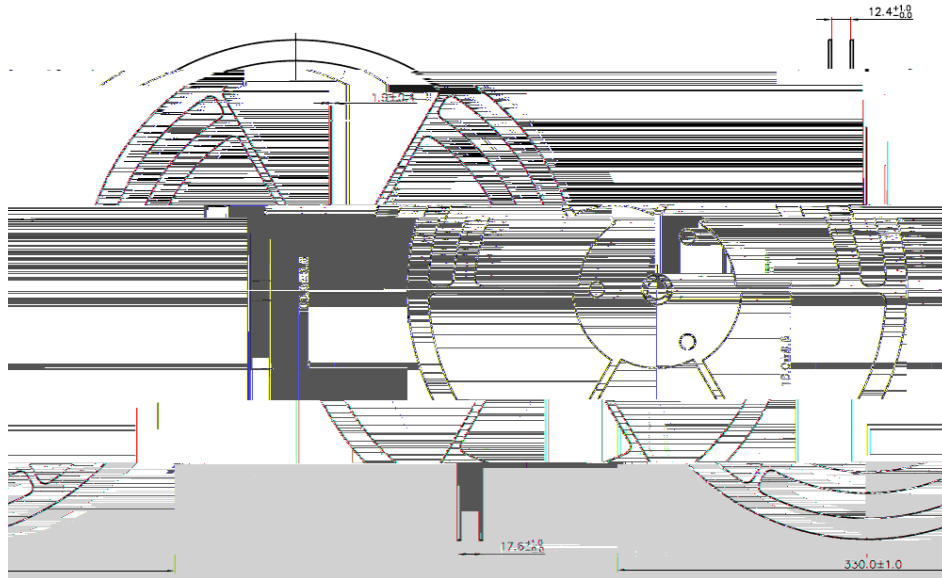


ESOP8/PP(95x130) Package Outline Dimensions

Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max.
A	1.300	1.700	0.051	0.067
A1	0.000	0.100	0.000	0.004
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
D1	3.050	3.250	0.120	0.128
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
E2	2.160	2.360	0.085	0.093
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

NOTE:

1. Drawing proposed to be made a JEDEC package outline MO-220 variation.
2. Drawing not to scale.
3. All linear dimensions are in millimeters.
4. Thermal pad shall be soldered on the board.
5. Dimensions of exposed pad on bottom of package do not include mold flash.
6. Contact PCB board fabrication for minimum solder mask web tolerances between the pins.



Device	Package	Package Drawing	Pins	MOQ
SCT9336STER	ESOP-8	STER	8	4000